UM10484

Integrated clean-up-PLL, TFF1xxxx and buffer amplifier

Rev. 3 — 10 October 2012 **User manual**

Document information

Info	Content
Keywords	External reference, clean-up-PLL, VCXO, LO generator, buffer amplifier, RF output power level, phase noise
Abstract	This document describes an integrated demonstration (demo) board for Clean-Up-PLL (CUP) local oscillator generator TFF11XXX/TFF100X. The demo board includes an output buffer amplifier based on BFU7XX series microwave transistors.

Revision history

Rev	Date	Description
v.3	20121010	Correct mistake in fig 4 and components in table 1.
v.2	20120202	Security status changed from company internal to company public.
v.1	20111221	Initial version.

Contact information

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1. Introduction

This user manual describes an integrated demonstration (demo) board for Clean-Up-PLL (CUP) local oscillator generator TFF11XXX/TFF100X. The demo board includes an output buffer amplifier based on the BFU7XX series of microwave transistors. Circuit schematics, a PCB layout design and test results are provided.

The demo board converts a reference signal (typically 10 MHz) to a frequency of 30 MHz to 50 MHz via a Xilinx CPLD and logic gate-based Voltage-Controlled eXternal Oscillator (VCXO). The fifth harmonic is filtered via a 7th-order Cauer filter and used as the reference for the TFF11XXX/TFF100X. Microwave transistors BFU7XX amplify the output of the TFF11XXX/TF100X to a level of 7 dBm, 10 dBm or 13 dBm, depending on the version of buffer used.

The NXP TFF11XXX, TFF1003, TFF1007, TFF1008 are a family of low phase-noise, high-frequency accurate microwave band Local Oscillator (LO) generators implemented in Silicon Germanium (SiGe) high Ft process. These devices have a combined frequency range of 7 GHz to 15 GHz, where:

- TFF1003/TFF1007/TFF1008 cover the VSAT Ku band (12 GHz to 14 GHz)
- TFF11XXX series cover the remaining frequency band

The LO generators require a reference input signal that minimizes the added phase noise to the LO generated signal. The Clean-Up-PLL generates an ultra-low phase noise reference signal based on a VCXO.

In practical applications, customers often use the LO generator to drive a mixer which could be a passive or active type. A high frequency buffer amplifier is required for applications requiring a higher LO drive level. The demo board has a wideband buffer amplifier designed to deliver an output power level of 7 dBm to 13 dBm.

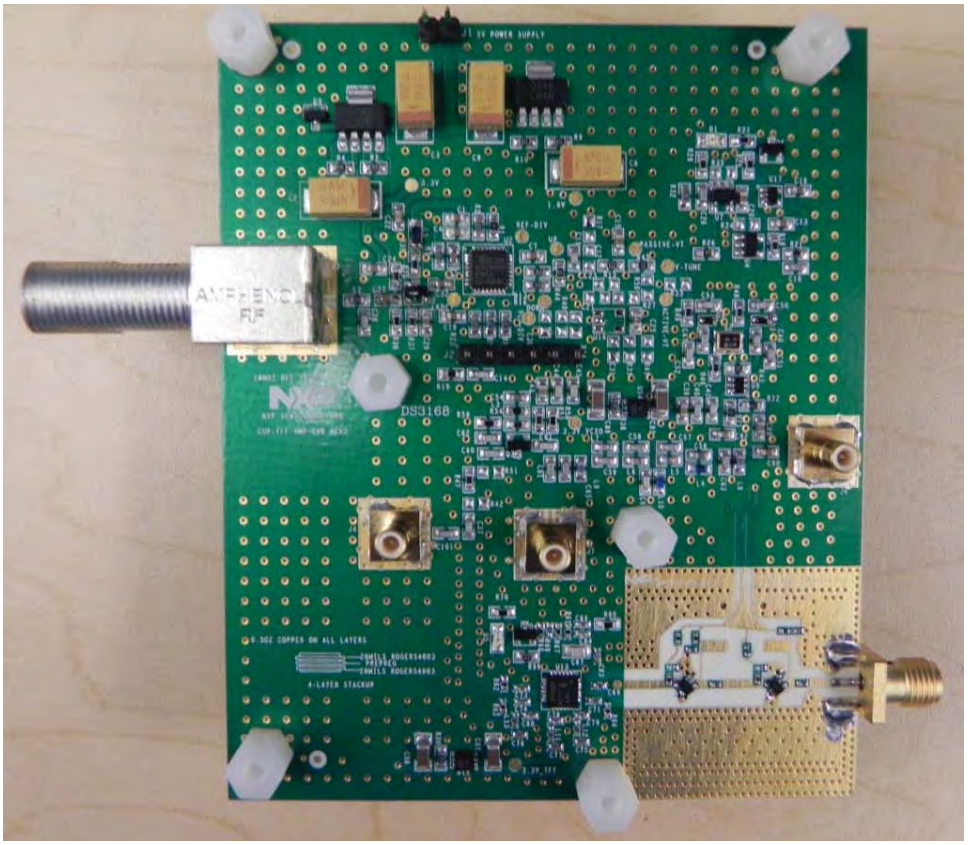

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Fig 1. PCB of integrated Clean-Up-PLL, TFF11XXX/TFF100X, and buffer amplifier

2. General description

2.1 High-level function review

The demo board accommodates additional customer-functional requirements with the following features:

Input: typically, a system may see a reference frequency of 10 MHz, which can be internal or external, however, a different reference frequency can be used. This demo board has a 10 MHz external reference input of 75 Ω with F-type connector for an input power level range of −15 dBm to +5 dBm.

Output: the demo board can provide an output power of 7 dBm, 10 dBm or 13 dBm to an output stage such as a mixer. The on-board buffer amplifier can be used, avoiding the need to design a separate circuit, saving engineering costs and time-to-market.

A high-level block diagram is shown in Figure 2.

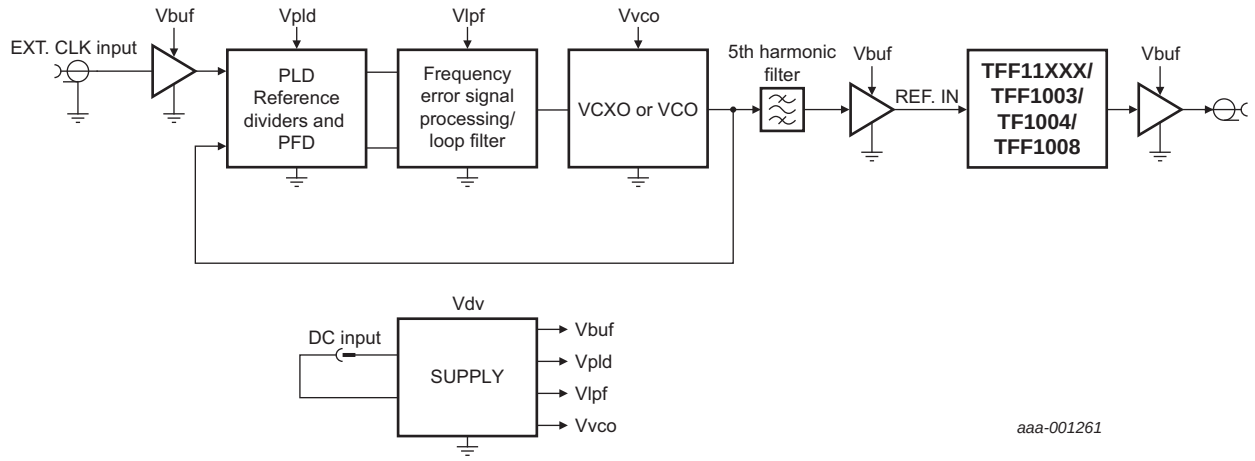

Fig 2. Block diagram of integrated Clean-Up-PLL, TFF11XXX/TFF100X, and buffer amplifier

2.2 Description of individual function blocks

External reference input: The external reference input provides the clock for the PLL. The amplifier converts this reference clock to a clipped sine wave that is recognized by the CPLD logic device.

Clean-Up-PLL: The Clean-Up-PLL for generating the required reference signal (CW) for the NXP LO generator family:

- TFF1003HN: for VSAT applications in the range 12.8 GHz to13.05 GHz
- TFF1007HN: VSAT applications at 14.75 GHz
- TFF1008 HN: VSAT application at 14.275 GHz
- TFF11XXX: frequency range 7 GHz to 15.2 GHz

The demo board has the following additional circuits to Clean-Up-PLL:

- External PLL lock detector: a simple voltage window detector logic circuit detects the tuning voltage at the loop filter output. A voltage between 0.4 V and 2.2 V indicates a Clean-Up-PLL locked status, and amber LED (D1) turns on.
- Phase-noise performance and tuning range can be optimized using an optional active loop filter which allows the customer to select specific components to implement either a passive or an active loop filter.
- Buffer amplifier: The buffer amplifier is the final stage which amplifies the TFF1XXX RF/microwave output signal from −4 dBm (typical) to +7 dBm to +13 dBm depending on the amplifier used.

3. Application board

3.1 Application circuit

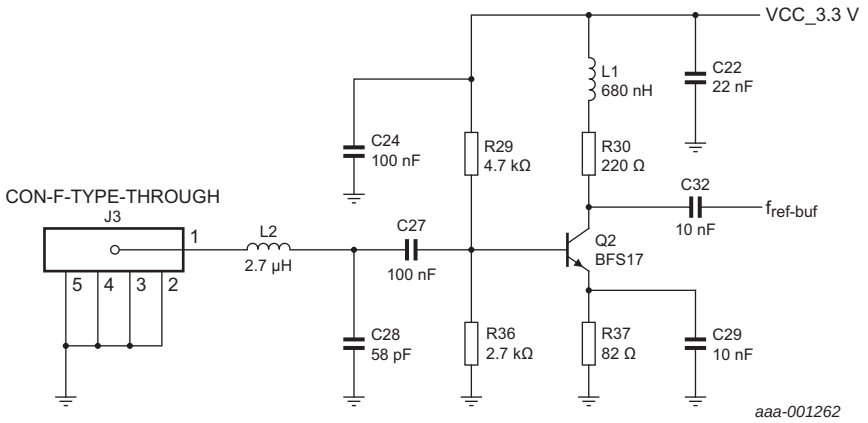

Fig 3. 10 MHz reference input and amplifier schematic

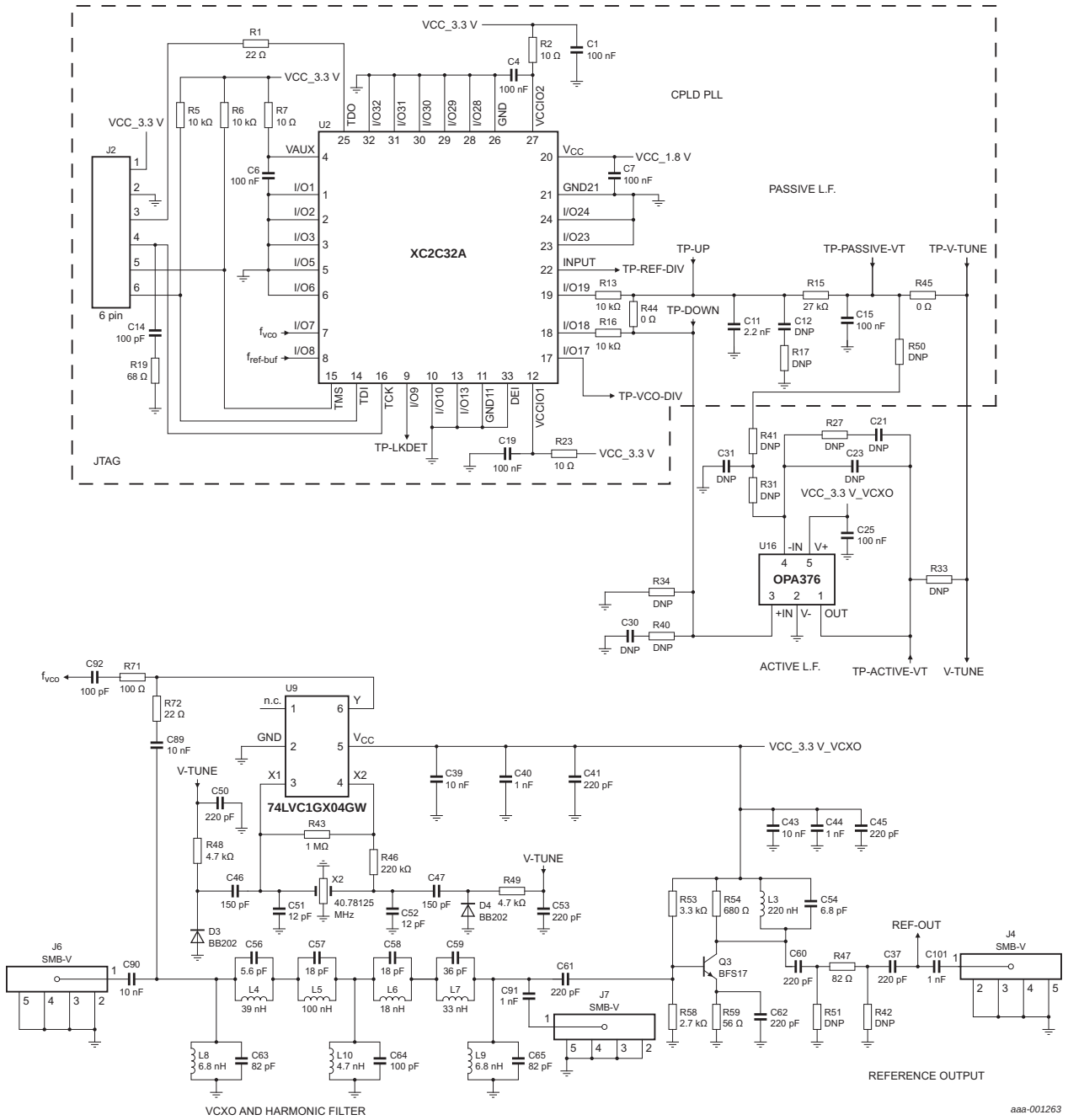

Fig 4. Clean-up-PLL schematic (part 1)

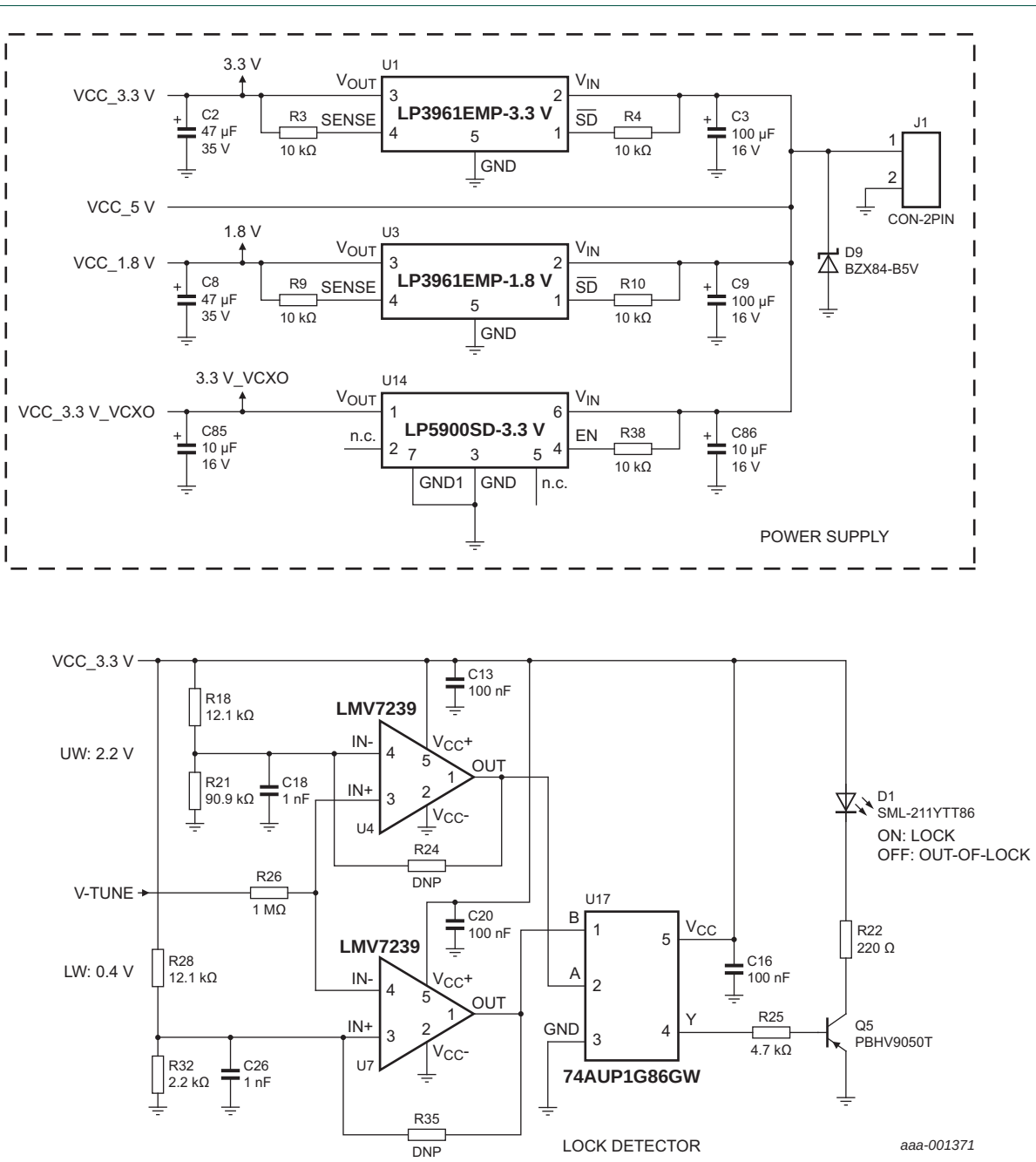

Fig 5. Clean-up-PLL schematic (part 2)

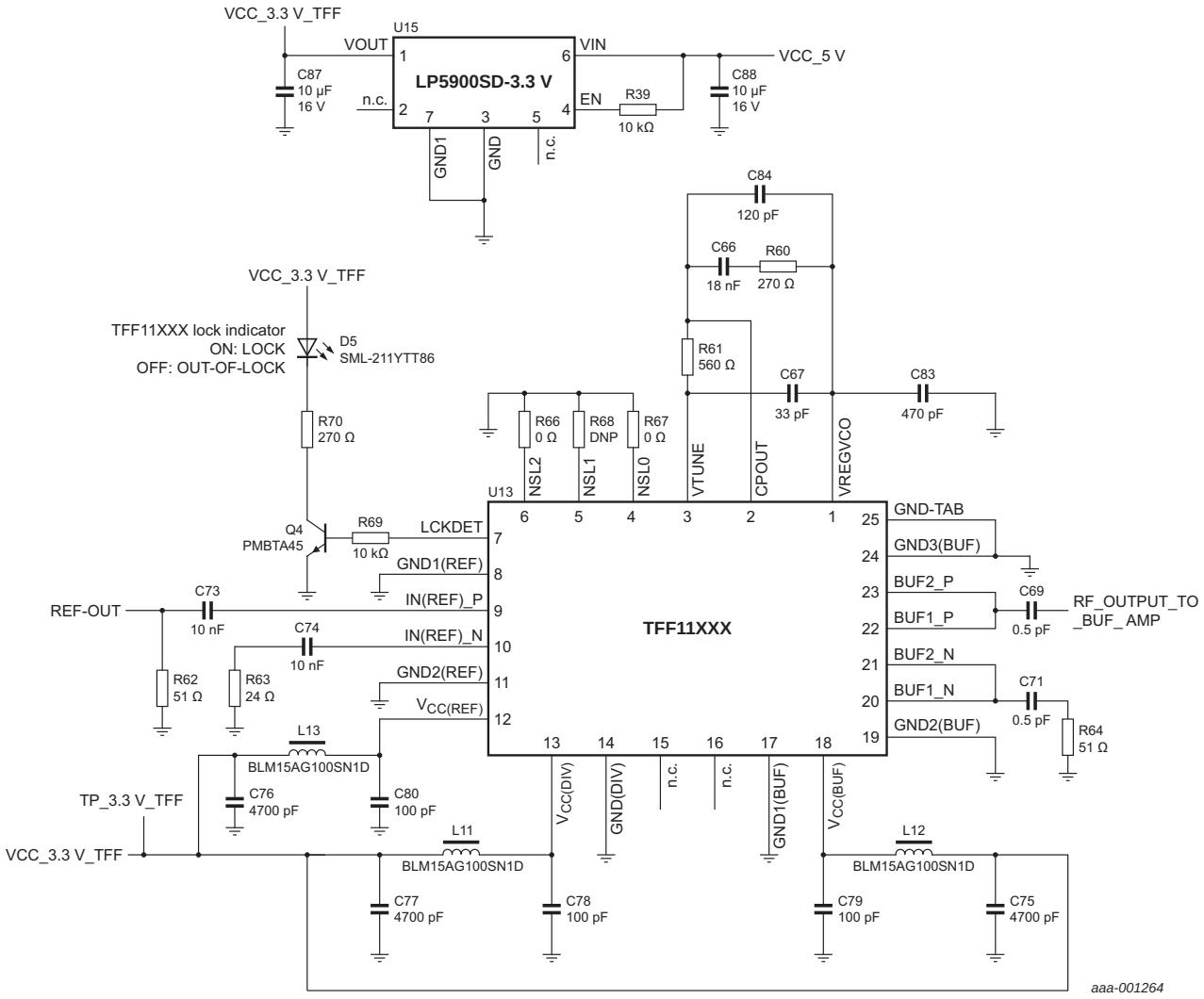

Fig 6. TFF100X/TFF11XXX schematic

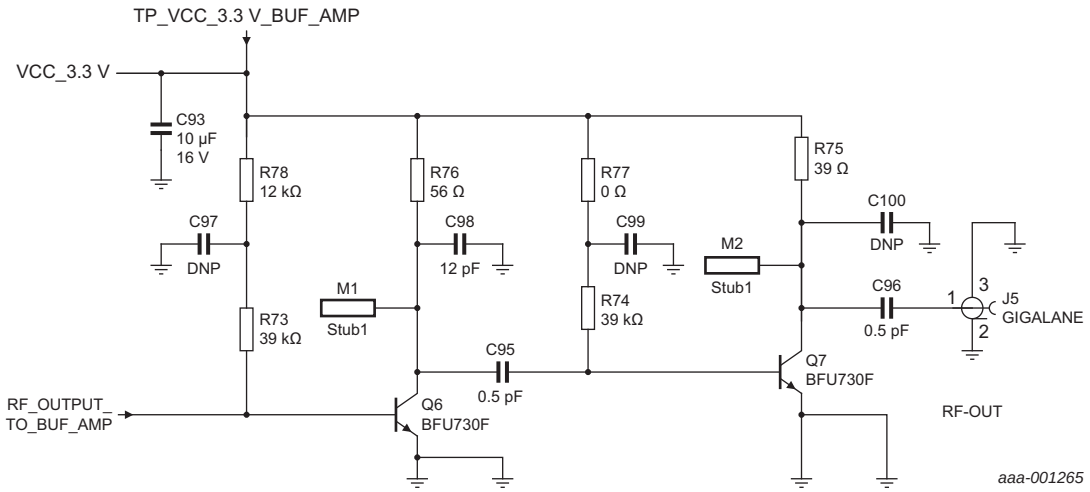

Fig 7. Buffer amplifier schematic (+10 dBm version)

3.2 Board layout

In general, a good PCB layout is an essential part of an RF circuit design. The demo board of the integrated clean-up-PLL, TFF100X/TFF11XXX and buffer amplifier can serve as a guideline or reference for laying out a board using this complete solution. Use controlled impedance lines for all high frequency inputs and outputs. Bypass V_{CC} with decoupling capacitors, preferably located as close as possible to the device. For long bias lines, decoupling capacitors may be required along the line farther away from the device. Proper grounding of the GND pins is also essential for good RF performance, either connecting the GND pins directly to the ground plane or through vias, or both.

Due to the nature of microwave signals, care is required to implement these circuits. Refer to the respective documents for layout recommendations and suggestions.

The material for this integrated board depends on the TFF100X/TFF11XXX and buffer amplifier which operate at microwave frequencies:

- Substrate: low-loss Rogers 4003
- Substrate critical thickness: 20 mils (0.508 mm)
- Dielectric constant: 3.38
- Dielectric Loss Tangent: 0.0025

The second substrate layer is solely for rigidity purposes. Figure 8 shows a detailed view of the layer stack-up.

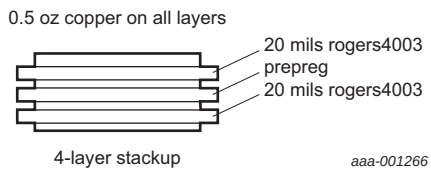

Fig 8. PCB stack-up of integrated clean-up-PLL, TFF11XXX/TFF100X, and buffer amplifier

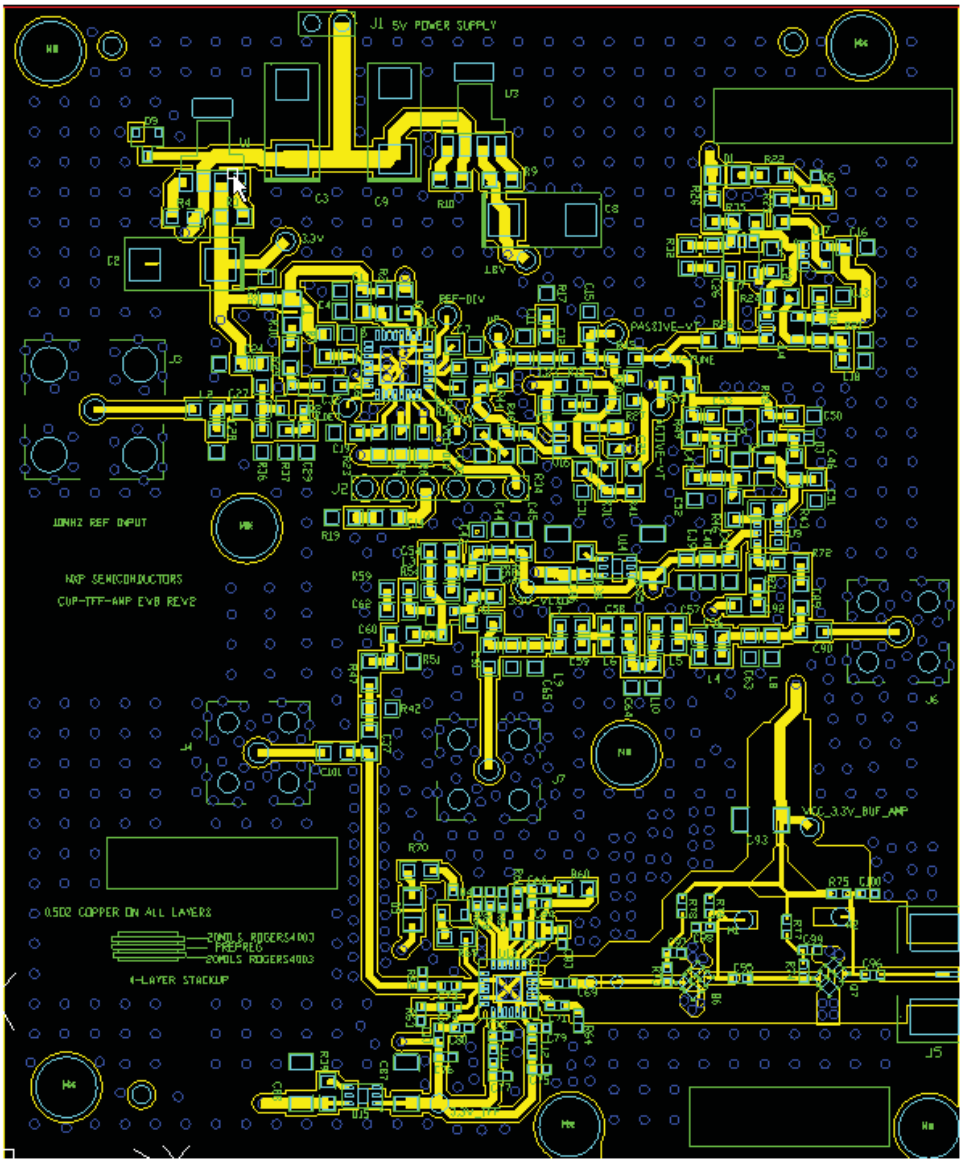

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Fig 9. Board layout of integrated clean-up-PLL, TFF11XXX/TFF100X, buffer amplifier (+10 dBm version)

3.3 Bill of materials

The Bill Of Materials (BOM) is determined by the required generated frequency. Because part of the PLL is a CPLD-based solution, it is possible to change the divider ratio (N and R) by software programming (JTAG).

PLL filter: flexible layout options allow different parts to be populated to make either a passive or an active loop filter.

A different crystal frequency may be required if the selected frequency is outside the pull-range limits (typically hundreds of ppm) of the VCXO.

Buffer amplifier components are also both frequency and output power level dependent. If the design requires an output power level of 7 dBm to 10 dBm at a frequency below 13 GHz, the output level is achieved by a cascaded BFU730 solution. If 10 dBm or more is required, a balanced amplifier solution is required to combine the two cascaded buffer amplifiers to achieve a higher output RF power to drive the mixer. Please contact NXP Semiconductors for reference design and evaluation board.

An example of a BOM for a VSAT BUC (Block-Up-Converter) application with a 13.05 GHz LO is given in Table 1.

For other frequency applications please contact NXP Semiconductors for technical assistance.

Table 1. Example BOM for a VSAT BUC with a 13.05 GHz LO

Quantity	Reference	Type	Manufacturer	Value
12	C1, C4, C6, C7, C13, C15, C16, C19, C20, C24, C25, C27	GRM188R71E104KA01D	Murata	100 nF
2	C2, C8	TAJE476K035RNJ	AVX	47 μF, 35 V
2	C3, C9	B45197A3107K509	EPCOS	100 μF, 16 V
1	C11	GRM1885C1H222JA01D	Murata	2.2 nF
8	C12, C21, C23, C30, C31, C97, C99, C100	<tbd>	Murata	DNP
3	C14, C64, C92	GRM1885C1H101JA01D	Murata	100 pF
6	C18, C26, C40, C44, C91, C101	GRM1885C1H102JA01D	Murata	1 nF
1	C22	GRM188R71C223KA01D	Murata	22 nF
1	C28	GRM1885C1H560JA01D	Murata	56 pF
6	C29, C32, C39, C43, C89, C90	GRM188R71H103KA01D	Murata	10 nF
8	C37, C41, C45, C50, C53, C60, C61, C62	GRM1885C1H221JA01D	Murata	220 pF
2	C46, C47	GRM1885C1H151JA01D	Murata	150 pF
2	C51, C52	GRM1885C1H120JA01D	Murata	12 pF
1	C54	GRM1885C1H6R8DZ01D	Murata	6.8 pF
1	C56	GRM1885C1H5R6DZ01D	Murata	5.6 pF
2	C57, C58	GRM1885C1H180JA01D	Murata	18 pF
1	C59	GRM1885C1H360JA01D	Murata	36 pF
2	C63, C65	GRM1885C1H820JA01D	Murata	82 pF
1	C66	GRM155R71C183KA01D	Murata	18 nF
1	C67	08051A330JAT2A	AVX	33 pF
4	C69, C71, C95, C96	GRM1555C1HR50CZ01	Murata	0.5 pF
2	C73, C74	GRM155R71C103KA01D	Murata	10 nF
3	C75, C76, C77	GRM155R71E472KA01	Murata	4700 pF

Table 1. Example BOM for a VSAT BUC with a 13.05 GHz LO *…continued*

Quantity	Reference	Type	Manufacturer	Value
3	C78, C79, C80	GRM1555C1H101JZ01	Murata	100 pF
1	C83	GRM155R71H471KA01D	Murata	470 pF
1	C84	GRM1555C1H121JA01D	Murata	120 pF
5	C85, C86, C87, C88, C93	C3216X7R1C106M	TDK	10 μF, 16 V
1	C98	GRM1555C1H120JZ01D	Murata	12 pF
2	D1, D5	SML-211YTT86	ROHM Semiconductor	SML-211YTT86
2	D3, D4	BB202	NXP Semiconductors	BB202
1	D9	BZX84-A5V1	NXP Semiconductors	BZX84-B5V
1	J1	90120-0762	Molex	CON-2PIN
1	J2	90120-0766	Molex	6PIN
1	J3	531-40047-4	Amphenol	CON-F-TYPE-THROUGH
3	J4, J6, J7	903-415J-51P	Amphenol	SMB-V
1	J5	PSF-S01-005	GigaLane	GIGALANE
1	L1	LQW21HNR68J00L	Murata	680 nH
1	L2	MLF1608A2R7K	TDK	2.7 μH
1	L3	B82496C3221J	EPCOS	220 nH
1	L4	LQW18AN39NJ00D	Murata	39 nH
1	L5	LQW18ANR10J00D	Murata	100 nH
1	L6	LQW18AN18NJ00D	Murata	18 nH
1	L7	LQW18AN33NJ00D	Murata	33 nH
2	L8, L9	LQW18AN6N8D00D	Murata	6.8 nH
1	L10	LQW18AN4N7D00D	Murata	4.7 nH
3	L11, L12, L13	BLM15AG100SN1D	Murata	BLM15AG100SN1D
2	M1, M2	PCB Copper	-	stub1
2	Q2, Q3	BFS17	NXP Semiconductors	BFS17
1	Q4	PMBTA45	NXP Semiconductors	PMBTA45
1	Q5	PBHV9050T	NXP Semiconductors	PBHV9050T
2	Q6, Q7	BFU730F	NXP Semiconductors	BFU730F
2	R1, R72	ERJ-3EKF22R0V	Panasonic - ECG	22 Ω
3	R2, R7, R23	ERJ-3EKF10R0V	Panasonic - ECG	10 Ω
11	R3, R4, R5, R6, R9, R10, R13, R16, R38, R39, R69	ERJ-3EKF1002V	Panasonic - ECG	10 kΩ
1	R15	ERJ-3EKF2702V	Panasonic - ECG	27 kΩ
13	R17, R24, R27, R31, R33, R34, R35, R40, R41, R42, R50, R51, R68	<tbd>	Panasonic- ECG	DNP
2	R18, R28	ERJ-3EKF1212V	Panasonic - ECG	12.1 kΩ
1	R19	ERJ-3EKF68R0V	Panasonic - ECG	68 Ω

Table 1. Example BOM for a VSAT BUC with a 13.05 GHz LO *…continued*

Quantity	Reference	Type	Manufacturer	Value
1	R21	ERJ-3EKF9092V	Panasonic - ECG	90.9 kΩ
3	R22, R30, R46	ERJ-2RKF2200X	Panasonic - ECG	220 Ω
4	R25, R29, R48, R49	ERJ-3EKF4701V	Panasonic - ECG	4.7 kΩ
2	R26, R43	ERJ-3EKF1004V	Panasonic - ECG	1 MΩ
1	R32	ERJ-3EKF2201V	Panasonic - ECG	2.2 kΩ
2	R36, R58	ERJ-3EKF2701V	Panasonic - ECG	2.7 kΩ
2	R37, R47	ERJ-3EKF82R0V	Panasonic - ECG	82 Ω
2	R44, R45	ERJ-3GEY0R00V	Panasonic - ECG	0 Ω
1	R53	ERJ-3EKF3301V	Panasonic - ECG	3.3 kΩ
1	R54	ERJ-3EKF6800V	Panasonic - ECG	680 Ω
1	R59	ERJ-3EKF56R0V	Panasonic - ECG	56 Ω
2	R60, R70	ERJ-3EKF2700V	Panasonic - ECG	270 Ω
1	R71	ERJ-3EKF1000V	Panasonic - ECG	100 Ω
1	R61	ERJ-2GEJ561X	Panasonic - ECG	560 Ω
2	R62, R64	ERJ-2GEJ510X	Panasonic - ECG	51 Ω
1	R63	ERJ-2GEJ240X	Panasonic - ECG	24 Ω
3	R66, R67, R77	CRCW04020000Z0ED	Vishay/Dale	0 Ω
2	R73, R74	ERJ-2GEJ393X	Panasonic - ECG	39 kΩ
1	R75	ERJ-2GEJ390X	Panasonic - ECG	39 Ω
1	R76	ERJ-2GEJ390X	Panasonic - ECG	56 Ω
1	R78	ERJ-3EKF123X	Panasonic - ECG	12 kΩ
1	U1	LP3961EMP-3.3	National Semiconductors	LP3961EMP-3.3
1	U2	XC2C32A-6QFG32C	Xilinx	XC2C32A
1	U3	LP3961EMP-1.8	National Semiconductors	LP3961EMP-1.8
2	U4, U7	LMV7239M5	National Semiconductors	LMV7239
1	U9	74LVC1GX04GW	NXP Semiconductors	74LVC1GX04GW
1	U13	TFF1003	NXP Semiconductors	TFF1003
2	U14, U15	LP5900SD-3.3V	National Semiconductors	LP5900SD-3.3V
1	U16	OPA376AIDBVT	Texas Instruments	OPA376
1	U17	74AUP1G86GW	NXP Semiconductors	74AUP1G86GW
1	X2	<tbd>	Tai-Saw	40.78125 MHz

Table 2. Example BOM matrix for different power and frequency applications

Power	Frequency (examples)			
	13.05 GHz	7 GHz	11.25 GHz	15 GHz
7 dBm	BOM1	BOM2	BOM3	BOM4
10 dBm	BOM5	BOM6	BOM7	BOM8
13 dBm	BOM9	BOM10	BOM11	BOM12

3.4 Evaluation equipment

The following equipment is required for evaluation tests.

- Low-noise DC power supply output to at least 500 mA at 5 V
- Precision ammeter to measure the supply current
- RF power meter capable of measuring up to 20 GHz or above
- Spectrum analyzer or signal analyzer with phase noise measurement feature capable of measuring up to 20 GHz or above
- 10 MHz reference input for an input power level range of −15 dBm to +5 dBm with the following phase-noise performance for divider N = 64:
  - 135 dBc/Hz at 1 kHz offset
  - 140 dBc/Hz at 10 kHz offset
  - 150 dBc/Hz at 100 kHz offset
- RF cables and connectors with minimum loss at 18 GHz or above

3.5 Connections and setup

The demo board has a few variants, so it is important to identify the frequency and RF power level of the demo board to be tested. Typically, the demo board is identified by suitable markings when it is fully assembled and tested. A step-by-step guide for operating and testing the demo board is as follows:

1. Connect the DC power supply to the V_{CC} and GND terminal at J1 which is a 2-pin terminal connector that can be clipped using a clip jacket.
2. Set the power supply to 5 V and current limiting to 400 mA.
3. Connect the RF output connector J5 to spectrum analyzer or power meter.
4. Turn on the power supply; the total current drawn must not exceed 300 mA.
5. LED D3 illuminates first, indicating that the TFF100X or TFF11XXX is in locked state. Locked state is indicated without a 10 MHz reference input due to the wide range of the TFF's reference input frequency. It is assumed that the free-running VCXO output is at the correct frequency, and at first lock. If the divider ratio is 64, it locks to the frequency of $64 \times f_{free\text{-}running\text{-}VCXO}$, but the Clean-Up-PLL is not locked until D1 illuminates.
6. Apply a 10 MHz reference input using a very low phase-noise source such as the OCXO module with F-type input connectors. LED D1 illuminates, indicating the Clean-Up-PLL is locked, and can be considered as a secondary lock ensuring the whole system is locked onto the 10 MHz reference input.
7. Test the phase noise and power of the Clean-Up-PLL which is the reference input of TFF100X/TFF11XXX at input J4.
8. Test the tuning voltage of the Clean-Up-PLL at test point VTUNE-PASSIVE if the loop filter is a passive type.
9. Test overall phase noise and power at output J5 with the spectrum analyzer and power meter.

4. Demo board typical measurement result

To demonstrate the performance of the integrated board, a representative board at 13.05 GHz for Ku band BUC is demonstrated in this document.

The following test result only refers to the final output performance of the demo board. For detailed test results of each individual building block, refer to the respective user manual, application note or data sheet.

For accurate measurement, use a suitable 10 MHz reference source in accordance with the requirements previously mentioned.

In the following test result, a Vectron OCXO module is used, part number 718Y-4153. Its phase noise plot is shown in Figure 10.

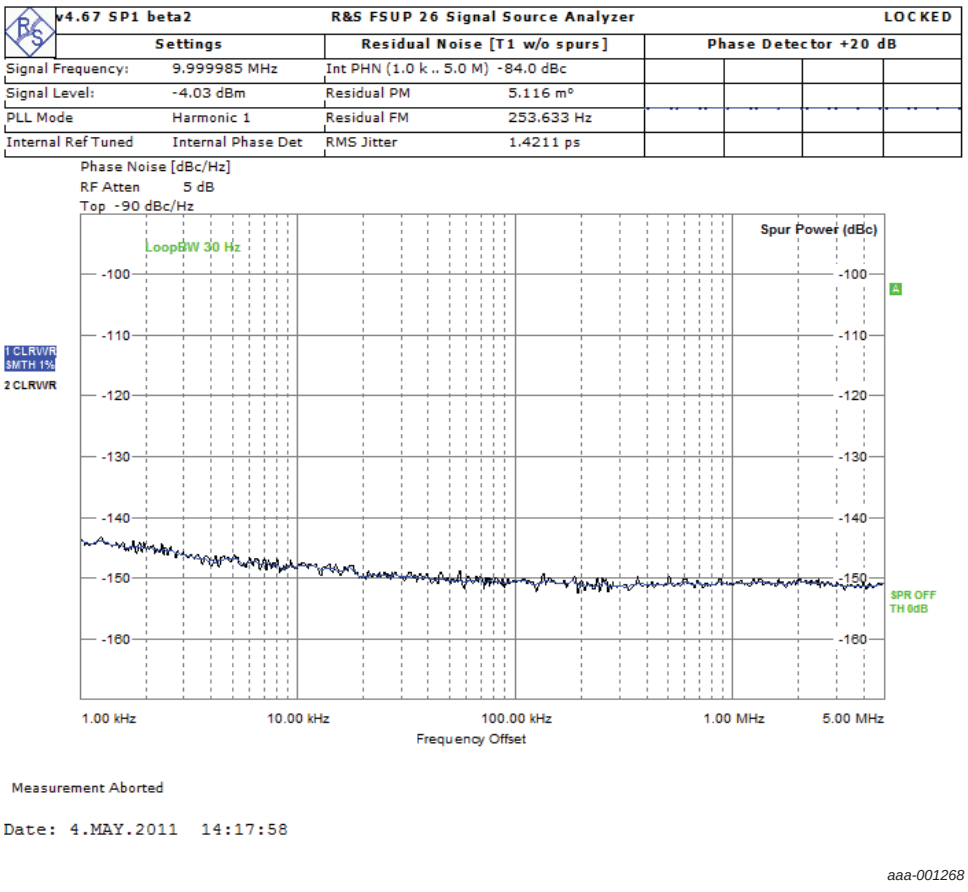

Fig 10. Reference input phase noise of a Vectron 10 MHz OCXO module

4.1 Demo board typical test result

f_{ref} input frequency = 10 MHz; P_{ref_in} input power level = 0 dBm.

Table 3. Typical results measured on the demo board

Test board example: 13.05 GHz for VSAT BUC; room temperature with 5 V power supply.

ID	Parameter	Conditions	Min	Typ	Max	Unit
1	current consumption		-	195	-	mA
2	phase noise out; see Figure 11	1 kHz offset	-	–96	-	dBc/Hz
		10 kHz offset	-	–102	-	dBc/Hz
		100 kHz offset	-	–101	-	dBc/Hz
		1 MHz offset	-	–108	-	dBc/Hz
3	spurious	reference	-	70	-	dBc
4	output power (13.05 GHz)	7 dBm version	-	7.1	-	dBm
		10 dBm version	-	9.8	-	dBm
		13 dBm version	-	13.2	-	dBm

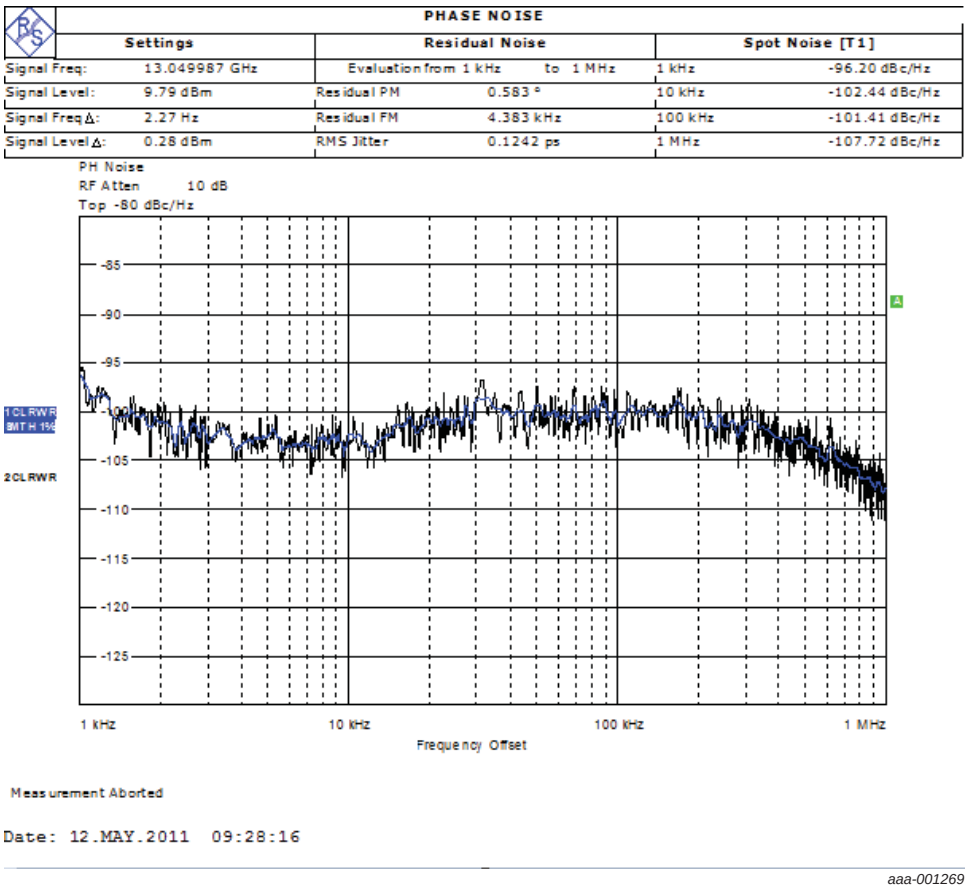

Fig 11. Phase noise and power output at 13.05 GHz (+10 dBm version)

5. Abbreviations

Table 4. Abbreviations

Acronym	Description
BOM	Bill Of Materials
BUC	Block-Up-Converter
CPLD	Complex Programmable Logic Device
CW	Continuous Wave
PLL	Phase-Locked Loop
OCXO	Oven-Controlled crystal Oscillator
PCB	Printed-Circuit Board
VCXO	Voltage-Controlled crystal Oscillator
VSAT	Very Small Aperture Terminal

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7. Contents

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